# Hot Spot Evaluation of Photovoltaic Modules

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## ABSTRACT

Hot-spot heating occurs in a photovoltaic (PV) module when its operating current exceeds the short-circuit current of a shadowed or faulty cell in a cell-string. This shadowed/faulty cell could overheat due to reverse bias and become a fire or electrical hazard. Currently, there are three different test methods used in the industry to identify and address this issue. These three methods are based on the UL 1703 (intrusive) standard, ASTM E2481-06 (non-intrusive) standard and IEC 61215 (non-intrusive) standard. Comparing and identifying the best test method [in terms of time, cost and complexity] is of great value to the consumers, PV module manufacturers and test laboratories such as ASU-PTL. The objective of this paper is to compare these three methods in order to identify the best test method for the modules composed of low and/or high shunt resistance cells. In this work, 18 modules composed of low and high shunt resistance cells were investigated in each of the test methods. Out of eighteen (9 mono-Si and 9 poly-Si) modules tested, sixteen modules (9 poly-Si and 7 mono-Si) passed the hotspot tests of all the three standards. The other two modules (mono-Si with voltage limited cells) passed in the ASTM and IEC methods, but failed in the UL method. These two failures in the UL method may be explained in terms of standard's worst-case assumption (open-circuited diodes) of non-sharing of the stress current by the installed bypass diodes of the modules and/or the extended test duration required in this standard.
**Keywords:** Hotspot, Safety, Qualification, Testing, Standards

## 1. INTRODUCTION

Photovoltaic (PV) modules consist of individual solar cells electrically connected together to increase their power output. For these modules, it's necessary to meet certain criteria for the determination of the reliability and safety. There are several test standards that provide test methods for testing these modules. Testing may need the modules to go through as many as 200 tests, few of them are for ensuring the performance, durability and few are related to safety issues of photovoltaic modules. Hot spot test is an important test to identify the reliability and safety issues related to the PV modules.

The most widely practiced standards for the hot spot test are: International Electrotechnical Commission IEC 61215 [1], Underwriters Laboratories UL 1703 [2] and American Standards for Testing and Measurements ASTM E2481-06 [3]. Some of the recent studies conducted by other research groups on this topic have been presented in various conferences [4-6]. All the three standards have their own test methods, advantages and disadvantages. A summary comparing these three standards is given in Table 1 below. The goal in this work is to identify the method which is more appropriate in terms of: testing duration, testing cost and identifying the real hot spot issues of production modules.

Table 1: Summary comparing between three standards for the hot spot test

| IEC | UL | ASTM |
|---|---|---|
| **Cell Selection Procedure:**<br>Finds the cell with the highest shunt resistance but there is no method specified for finding the localized shunt or lowest shunt resistance, which may be most dangerous.<br><br>The selection of highest shunt resistance being done by shade and un-shade every cell and measure the Isc, the cell with highest difference between Isc is the cell in concentration (if there are multiple cells, the cell close to centre is selected) | **Cell Selection Procedure:**<br>In this test, the leads are attached to at least 10 cells selected at random. From the 10 cell sampling it does require selection of both the highest and lowest shunt resistance cells, but of course there is a reasonable likelihood of not selecting the potential small population of cells with localized shunts that can cause hot spot problems if used in high voltage systems.<br><br>The selection of cells i.e. highest, lowest and medium resistance being done with the help of dark I-V test, where reverse voltage is applied on the cell in dark conditions and measure the I-V characteristics | **Cell Selection Procedure:**<br>In this test procedure, it is necessary to get I-V curves of module by shading every individual cell and select the cells with highest (1) and lowest (3) resistance.<br><br>I-V curves in STC for every cell by shading it completely. |
| **Assumption of Installed Diode:**<br>In this case a bypass diode is always connected with the cells in module and full shadowing will also not affect the short circuit current at all as one of the diodes will turn on and carry the current around the shadowed cell. The diode will maintain the current flow through the module at Isc even when a cell is shaded | **Assumption of installed Diode:**<br>Absence of bypass diodes in the production modules is assumed in this test method. This test method simulates an extreme fault condition wherein a cell is forced to operate in reverse-voltage hot spot heating at the module's maximum power point. Since all the high power commercial modules have pre-installed diodes, this fault condition could occur if all the diodes fail in the open-circuit condition. | **Assumption of Installed Diode:**<br>Like the IEC standard, here also bypass diode comes into picture (connected with cells) but the I-V measurements give a clearer pattern for selecting the appropriate high- and low-shunt resistance cells |
| **Stress Testing Procedure:**<br>The procedure in this test involves a total test time of five (5) hours in one hour increments with having a cell fully shadowed (in STC). It has been experimentally proven that type A cells have failed after a longer time period, so the time in not enough. | **Stress Testing Procedure:**<br>This procedure involves of total 100 hrs of reverse biasing with power supply as well as heating of cell with IR light (for voltage limited cells) or light illumination for maximum power dissipation (for current limited cells) | **Stress Testing Procedure:**<br>In this procedure, there are 3 cells selected with lowest shunt resistance (localized) and get them heated with worst case heating (the maximum part shaded in this case) for 1 hr for every cell (total 3 hrs).<br>The cell with highest shunt resistance gets heated with minimum part shaded for ~50 hrs at irradiance 800-1200 W/m $^{2}$ |
| **Testing Cost and Time:**<br>The cost and time associated with this test is the lowest. | **Testing Cost and Time:**<br>The cost and time associated in much higher and risk of selecting the appropriate cells is also there as we can select the best and worst cell only from randomly selected 10 cells. Moreover, this intrusive test method is not suitable for the production modules as the cells need to be individually accessed during the testing. | **Testing Cost and Time:**<br>The time consumed in this test is lower than UL, if done with simulator. Cost is lower than UL hot spot test. This procedure gives the best cell selection approach and then stressing the selected cells (small number but longer duration for high resistance cells and large number but shorter duration for low resistance cells). |

# 2. METHODOLOGY

As shown in Table 2, a total of 18 modules were tested in this test program with three sets of poly-Si modules from three different manufacturers (A, B, C) and another three sets of mono-Si modules from three different manufacturers (D, E, F). The design type of each module within a set was identical.

Table 2: Eighteen Test Modules – 9 poly-Si modules from three different manufacturers and 9 mono-Si modules from three different manufacturers

| Standard | Poly-Si | | | Mono-Si | | |
|---|---|---|---|---|---|---|
| IEC 61215 | Poly #A | Poly #B | Poly #C | Mono #D | Mono #E | Mono #F |
| ASTM E 2481-06 | Poly #A | Poly #B | Poly #C | Mono #D | Mono #E | Mono #F |
| UL 1703 | Poly #A | Poly #B | Poly #C | Mono #D | Mono #E | Mono #F |

All the eighteen modules were tested according to the procedures of the three standards (6 modules for each standard): IEC 61215, UL 1703 and ASTM E2481. A summary of these procedures is provided below.

## 2.1 Procedure of IEC 61215

As per the procedure of IEC 61215, for cell selection, completely shadow each cell in turn and select the cell which gives the largest decrease in short-circuit current when shadowed. During this process, the irradiance shall not change by more than ± 3 %, the one resulting in the largest decrease in short-circuit current is selected as the test cell.
If there is no cell in parallel string the

$$Isc\ (*) = Imp$$

and if there is any cell in parallel string the

$$Isc\ (*) = Isc * (p - 1)/p + (Imp / p)$$

Where
Isc is the short-circuit current of the unshadowed module;
Imp is the current at maximum power of the unshadowed module;
p is the number of parallel strings in the module.

Here if Isc(*)is less than Isc of module, the shading of selected cell will be 100 % for the actual stress; otherwise, the shading will be done with the help of cell shading program. In the cell shading program, the worst case shadowing of selected cell is chosen by gradually decreasing the shadowed area of the selected cell until Isc of the module coincides as closely as possible with Isc (*). In this condition, the maximum power is dissipated within the selected cell. Later Non intrusive hotspot endurance test proceeds for 5 hrs light exposure. The requirements for IEC are [1]:

1. Irradiance must be 1000 W/$m^2$ $\pm$ 10%.
2. Wind speed must be less than 2 m/s.
3. Module temperature must be 50 $^\circ C$ $\pm$ 10%.

Later the module must go through visual inspection test, insulation test and electrical performance tests following IEC 61215 as pass criteria.

## 2.2 Procedure of UL 1703

In this procedure selection of the cells (susceptible) is done with the help of dark current and voltage (I-V) characteristics of each cell (all 10 cells) is measured. Three cells (test cells) are selected based on highest, median, and lowest effective shunt resistance (as found from the dark I-V curves). The test cells are driven with power supplies and possibly a light source so that they dissipate the maximum amount of power based on the module's cell configuration. This test proceeds for 100 cumulative hours of maximum power dissipation in one hour intervals followed by a resting time where the cell is allowed to cool to within 10°C from ambient. Here standard gives different patterns of testing for different types of cells; if the cell is voltage limited applied will be maximum voltage ($V_L$ = N * Vmp), where N is number of series cells per bypass diode to the cell and light illumination that can provide maximum power dissipation as well as IR lights for heating up the cell(s) at Nominal Operating Cell Temperature (NOCT). If the cell is current limited applied will be maximum current ($I_L$ = Isc) with the cell heat-up with the help of IR light at Nominal Operating Cell Temperature (NOCT). The flame, burn, any damage, crack must be reported [2].

### 2.3 Procedure of ASTM E2481-06

This method selects three lowest and one highest resistance cells from the current and voltage characteristics. These I-V characteristics can be found by shading every cell in turn. After selecting 3 lowest resistance cells, find the worst case shading by matching the worst case shadowing condition occurs when the "kink" in the I-V curve of the shadowed module coincides with Imp. Shade the cell at worst case shadowing and expose the module to the illumination source. Irradiance must be between 800 and 1200 $Wm^{-2}$ for one hour [3]. Follow the same procedure for remaining two cells. Then find the worst case shadowing of cell with highest resistance by following the same procedure as it was for lowest resistance cells. After selecting the worst case shadowing, shade the cell at worst case shadowing and expose the module to the illumination source. Irradiance must be between 800 and 1200 $Wm^{-2}$. Total radiant exposure reaches 180 $kJm^{-2}$. (This is equivalent to 50 hours at 1000 $Wm^{-2}$). The module later must go through insulation test, visual inspection test and electrical performance tests as per ASTM.

## 3. RESULTS AND DISCUSSION

The results obtained in this work are presented in two sub-sections: Polycrystalline Silicon and Monocrystalline Silicon. An overall discussion on all the test results is presented in the last sub-section.

### 3.1 Results of Poly-Si Modules

The concluding remarks on the results obtained for all the nine poly-Si modules are presented in Table 3. The results obtained for the individual standard are briefly presented below.

All the three poly-Si modules have met the post-test requirements of the IEC 61215 hotspot test which include: visual inspection, insulation test and electrical performance test. All the three poly-Si modules have met the post-test requirements of the UL 1703 hotspot test which include the absence of fire, smoke or visual defects. All the three poly-Si modules have met the post-test requirements of the ASTM E2481-06 hotspot test including visual inspection, insulation test and electrical performance test. Therefore, it is concluded that all the nine poly-Si modules have passed the hotspot test requirements of all the three standards. It may be noted that the shading area during the stress testing per ASTM standard varied a lot from the lowest-

resistance cell to the highest-resistance cell depending on the manufacturer. As an example, for manufacturer A module, the average shading of lowest resistance cells was 31% and the worst case shading of highest resistance cell was 17.7%.

Table 3: Hotspot failure summary of poly-Si modules in IEC, UL and ASTM standards testing

| Manufacturer | IEC 6215 | UL 1703 | ASTM E2481-06 |
|---|---|---|---|
| A | Pass | Pass | Pass |
| B | Pass | Pass | Pass |
| C | Pass | Pass | Pass |

### 3.2 Results of Mono-Si Modules

The concluding remarks on the results obtained for all the nine mono-Si modules are presented in Table 4. The results obtained for the individual standard are briefly presented below.

Table 4: Hotspot failure summary of mono-Si modules in IEC, UL and ASTM standards testing

| Manufacturer | IEC 61215 | UL 1703 | ASTM E2481 |
|---|---|---|---|
| D | Pass | Fail (failed after 70 hours of stress testing; all are voltage limited cells) | Pass |
| E | Pass | Fail (failed within 5 minutes of stress testing; all are current limited cells) | Pass |
| F | Pass | Pass (all are voltage limited cells) | Pass |

All the six mono-Si modules have met the hotspot requirements of IEC 61215 and ASTM E2481-06 standards. Two of the three mono-Si modules (manufacturers D and E) tested per UL 1703 method did not meet the requirements of the standard. After performing intrusive hotspot test according to UL 1703, the smokes and front glass shattering were observed on one module (manufacturer E). These failures (see Figure 1) were observed within the first few minutes (less than 5 minutes) of the stress testing. All the cells of this module were determined to be current limited cells and two of the ten selected cells (low and median resistance cells) failed in this test. The other failure occurred with manufacturer D module. All the cells of this module were determined to be voltage limited. A burn mark was found on the front surface of a cell; however, it didn't smoke or shatter the glass (see Figure 2).

Figure 1: Hotspot failure leading to smoke and front glass shattering
within 5 minutes of stress testing per UL 1703 standard (Manufacturer E)

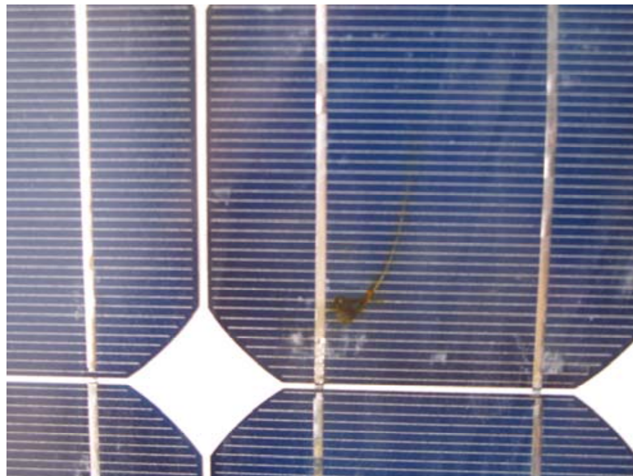

Figure 2: Hotspot failure leading to a burn mark
After more than 70 hours of stress testing per UL 1703 standard (Manufacturer D)

### 3.3 Discussion

The IEC method finds the cell with the highest shunt resistance, which is actually less susceptible to hotspot heating failure because of uniform distribution of heat throughout the cell and of insufficient duration (5 hours) of stress testing. Unless all the cells in the module are low shunt resistance cells, it appears that the IEC method would not be able to lead to a hot spot failure. The UL 1703 method finds the cell with both type of shunt resistances but it can be done out of 10 randomly selected cells only. Since the standard requires for 10 electrically accessible cells and finds the worst case cells out of these 10 cells, there is very high

possibility of not selecting the failure susceptible cells during the random selection. The other aspect of this test is stressing the cell without taking the bypass diode in circuit into account, which is not the case in real module. When module is installed in real field bypass diode is always present in the circuit in order to reduce excessive heating by sharing the current between the shaded cell string and diode. Moreover, this intrusive method is not suitable to the periodical testing of production modules though this method is of great value for determining number of cells per diode during the pre-production design stage of the modules. The ASTM method systematically (not randomly as in UL 1703 method) selects both the highest and lowest shunt resistance cells and stresses the selected cells appropriately. Lowest resistance cell is highly susceptible to quick failure due to high current heating in a localized area. The ASTM selects the 3 lowest resistance cells and stresses each of them for 1 hour at 1000 W $m^{-2}$ and it appears to be enough time to cause failure in the lowest resistance cells or current limited cells. On the other hand, the ASTM method selects one highest resistance cell which is less susceptible to failure in a short period time because of uniform heat distribution throughout the cell. Since short duration stressing is not enough for high resistance cells, the ASTM method provides longer time of stressing with 50 hours of irradiance at 1000 W $m^{-2}$ or the cell is exposed to 180 kJ $m^{-2}$ of light. Based on the limited testing conducted per IEC, UL and ASTM methods in this work, the ASTM method appears to be the best method for systematic finding of the hotspot cells and appropriately stressing the worst case cells (highest and lowest shunt resistance) of the production modules.

None of the poly-Si modules failed in any of the three test methods. Out of nine mono-Si modules, two of them failed in the UL 1703 test but not in the IEC and ASTM methods. The reason for failing manufacturer D module (current limited) in the UL test but not in the IEC and ASTM tests could be possibly explained as follows. In the UL method, the entire string current shall be flowing through the stressed cell whereas in the ASTM and IEC methods the current is shared by both stressed cell and the by-pass diode attached to the module. But if one compares with the production modules, there is always bypass diodes connected to strings which can partly/mostly dissipate the heat by passing the current through the diodes. The reason for module E (voltage limited cell) failing in the UL method could be attributed to absence of current sharing by the diodes and the longer duration (more than 70 hours) of stressing as compared to 5 hours (IEC) and 50 hours (ASTM). It may be necessary to extend the stress time of ASTM method to 100 hours (like in the UL method) to ensure that the voltage limited cells do not fail even after long stress testing.

## 4. CONCLUSIONS

In this work, all the three (IEC, UL and ASTM) test methods were investigated with 18 modules composed of low and high shunt resistance cells. Out of 18 (9 mono-Si and 9 poly-Si) modules tested, 9 poly-Si and 7 mono-Si modules passed the hotspot tests of all three standards. Both failures (mono-Si with voltage limited and current limited cells) occurred in the UL method. One failure occurred within the first few minutes (current limited) and the other failure occurred about 70 hours of stress (voltage limited). The IEC 61215 method was found to be the most economical method in terms of test duration but the issue with this method is that it selects only the cell with the highest shunt resistance for the stress testing. The highest shunt resistance cell has the characteristics of uniform heating and this uniform heat distribution minimizes the hot spot failure during the stress testing duration warranted by the IEC 61215 standard. Another reason for the absence of hot spot failure in this test method could be due to the current sharing by both the stressed cell and bypass diode attached to the cell string. The UL 1703 standard calls for a good cell screening method on limited (only ten) randomly selected cells (there is a high likelihood of not selecting the worst cell) to identify the low, median and high shunt resistance cells; however, this method requires the construction of a special test module and also the periodic testing of production modules is not practical. The other issue with this method is completely neglecting the current sharing task of the bypass diodes. In actual production modules, there are always bypass diodes connected in the circuit. This bypass diode shares the current/heat of the

stressed cell of the string and reduces the hot spot failure of the cell. Since the UL 1703 method stresses the individual cells without any bypass diode, it may be viewed that this test method causes undue failure or the worst case failure if the diodes are assumed to fail in the field under open-circuit modes. The ASTM E2481-06 method appears to be the best method for accurate cell selection and stress testing procedures. The results obtained after performing tests on 18 modules indicate that none of the modules failed in this test method. The reason for the absence of hot spot failure in the ASTM method but the presence of hot spot failure in the UL method could be potentially attributed to the presence of bypass diode in the test module used in the ASTM method, which bypasses the current and partly shares the heat dissipated in the cell. The stress testing duration of the ASTM method may be extended beyond 50 hours to match with 100 hours of the UL method. In this work, only a limited number of modules (18) have been tested. It is intended to continue this work with a large number of modules to ensure that the results and conclusions obtained in this short study are statistically valid.

## REFERENCES

[1] International Electrotechnical Commission (IEC) 61215, "Crystalline silicon terrestrial photovoltaic (PV) modules - design qualification and type approval", pp. 55-64 (2005)

[2] Underwriters Laboratory (UL) 1703, “Standard for Flat-Plate Photovoltaic Modules and Panels”, pp 51-57 (2004)

[3] American Standards of Testing and Measurements (ASTM) E2481, “Standard Test Method for Hot Spot Protection Testing of Photovoltaic Modules” (2006)

[4] Wohlgemuth, J. and Herrmann, W., “Hot Spot Test for crystalline silicon modules”, IEEE Photovoltaic Specialists Conference, pp. 1062- 1063 (2006)

[5] Herrmann, W., Wiesner, W., and Vaasen, W., “Hot Spot Investigation on PV Modules - New Concepts for a Test Standard and Consequences for Module Design with Respect to Bypass Diode”, IEEE PV conference , pp. 1129-1132 (1997)

[6] Herrmann, W., Alonso, M., Boehmer, W. and Wambach, K., “Effective Hot-Spot Protection of PV Modules - Characteristics of Crystalline Silicon Cells and Consequences for Cell Production”,17th European Photovoltaic Solar Energy Conference, Munich (2001)